

ST755 by T. Sampieri & F. Lentini - S

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ADJUSTABLE, INVERTING, NEGATIVE OUTPUT, CURRENT MODE PWM REGULATOR

The ST755 is an adjustable, inverting switch-mode DC-DC regulator with an internal Power MOSFET that generates an adjustable negative output from a positive voltage input of 2.7V to +11V.

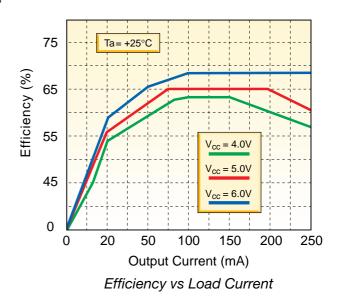
The output current is guaranteed at 200mA (for $V_{in} > 4.5V$, $V_{out} = -5V$ and 0°<Ta<70°C) and 275mA (typical value at Ta = 25°C, Vout= -5V).

A logic controlled shut down pin that interfaces directly with a microprocessor reduces the supply current to only 10μ A. The input to output differential voltage is limited to Vin+lVoutl<12.7V. Without any load the supply current is only 1.2mA. The device is supported by an application demoboard that can be used for evaluation. The printed circuit layout of the demoboard can be copied directly or incorporated into the customer's application board.



FEATURES

- 2.7V to 11V input to adjustable negative output conversion
- 1W guaranteed output power (V_{in}>4.5V)
- > 68% typ. efficiency
- Very low quiescient current:
 1.2mA in on mode
 - $10\mu A$ in shut down mode
- Soft start
- Very low noise output
- > 160KHz fixed- frequency oscillator
- Mixed bipolar-CMOS technology



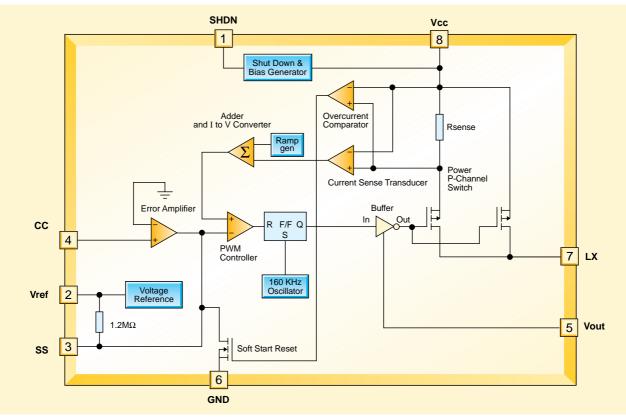
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Block diagram of ST755

APPLICATION INFORMATION

The ST755 is an IC developed for voltage conversion from an input voltage ranging from +2.4V to 11V to a regulated adjustable negative output limited by:

 $|Vout| \le 12.7V - V_{in}$

For greater efficiency, high stability and low noise performance the circuit adopts a current-mode PWM control scheme.

BCD TECHNOLOGY

This device has been developed in BCD technology in order to achieve: high temperature stability, the best REFERENCE precision, a very low quiescent current and jitter free operation. The final stage is built around a 0.7Ω , 2Amp P-Channel Power MOSFET.

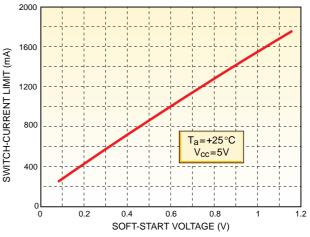
A fraction of the output current is used for current detection.

Internal clock frequency is fixed to 160KHz.

SOFT-START (SS pin)

Soft-Start input is a voltage dependent on the Output Current limit.

Applying an appropiate capacitor at the SS input it is possible to obtain a soft-start current limitation during power up. When SHDN input is low, the total current consumption is reduced to 10µA.



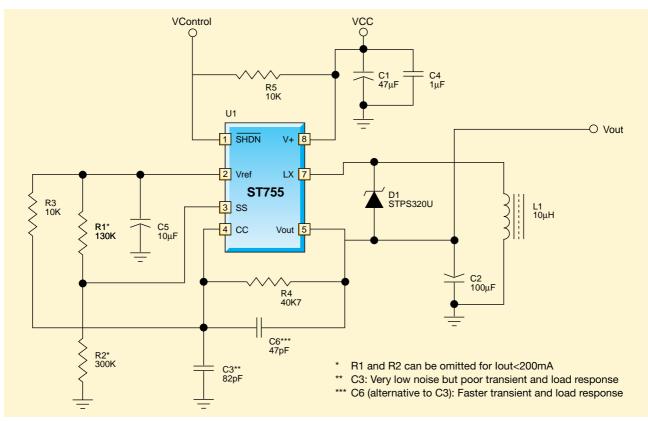
Switch-current limit vs soft-start voltage



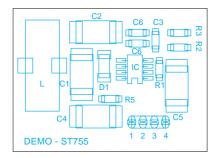


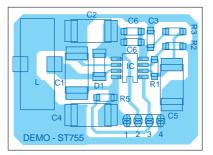
APPLICATION CIRCUIT

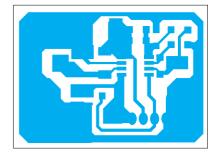
To achieve the best performance from switching power supply topology, particular care must be taken in the drawing of the layout. The layout design proposed on the suggested demoboard helps shorten the developing time, while minimising EMI, and obtaining low noise and jitter free operation.



Typical switching power supply application circuit of ST755







PIN CONFIGURATION O	OF DEMOBOARD
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PIN	DESCRIPTION	
1	V _{cc}	
2	V _{out}	
3	SHDN	
4	GND	

CAPACITOR	VALUE	RESIST.	VALUE
			KΩ
C1	47μF	R1	130
C2	100µF	R2	300
C3	82pF	R3	10
C4	1μF	R4	40.7
C5	10µF	R5	10
C6	47pF	-	-

